IN THE CLAIMS

1. (withdrawn) A method for fabricating a semiconductor device using an ArF exposure light source, comprising the steps of:

forming a conducting layer on a semiconductor substrate;

forming a first hard mask layer, a second hard mask layer and a third hard mask layer on the conducting layer in order;

forming a photoresist pattern on the third hard mask layer using an ArF exposure light source in order to form a predetermined patter;

forming a first hard mask pattern by etching the third hard mask layer using the photoresist pattern as an etching mask;

forming a second hard mask pattern by etching the second hard mask layer using the first hard mask pattern as an etching mask;

removing the first hard mask pattern; and

etching the first hard mask layer and the conducting layer using the second hard mask pattern as an etching mask and forming a stacked hard mask pattern having the conducting layer and the second and first hard mask patterns.

2. (withdrawn) The method in accordance with claim 1, wherein the first hard mask layer is a doped polysilicon layer or an undoped polysilicon layer.

3. (withdrawn) The method in accordance with claim 1, wherein the second hard mask layer is an oxynitride layer or a silicon nitride layer.

4. (withdrawn) The method in accordance with claim 1, wherein the third hard mask layer is the same materials as the conducting layer.

5. (withdrawn) The method in accordance with claim 1, wherein the third hard mask layer is etched by an SC-1 ($NH_4OH:H_2O_2:H_2O$=1:4:20) solution.

6. (withdrawn) The method in accordance with claim 1, wherein the first hard mask layer has a thickness in a range of 50 Å ~ 100 Å

7. (withdrawn) The method in accordance with claim 1, wherein the predetermined pattern is a gate electrode pattern, a bit line pattern or a metal line pattern.

8. (withdrawn) A method for fabricating a semiconductor device using an ArF exposure light source, comprising the steps of:

forming a conducting layer on a semiconductor substrate;

forming a first hard mask layer, a second hard mask layer and a third hard mask layer on the conducting layer in order;

forming a photoresist pattern on the third hard mask layer using an ArF exposure light source in order to form a predetermined patter;

forming a first hard mask pattern by etching the third hard mask layer using the photoresist pattern as an etching mask;

etching the second hard mask layer and the first hard mask layer using at least the first hard mask pattern and forming a triple stacked hard mask pattern having the first hard mask pattern, a second hard mask pattern and a third hard mask pattern; and

etching the conducting layer using triple stacked hard mask pattern as an etching mask and simultaneously removing the first hard mask pattern, whereby a stacked structure having the conducting layer, the second hard mask pattern and the third hard mask pattern is formed.

9. (withdrawn) The method in accordance with claim 8, wherein the first hard mask layer is a LPCVD oxynitride layer and the second layer is a PECVD oxynitride layer.

10. (withdrawn) The method in accordance with claim 8, wherein the second hard mask layer is twice or more times as thick as the first layer.

11. (withdrawn) The method in accordance with claim 8, wherein the third hard mask layer is the same materials as the conducting layer.

12. (withdrawn) The method in accordance with claim 8, further comprising the step of forming an antireflective coating layer on the third hard mask layer.

13. (original) A method for fabricating a semiconductor device using an ArF exposure light source, comprising the steps of:

forming a conducting layer on a semiconductor substrate;

forming a first hard mask layer and a second hard mask layer on the conducting layer in order;

forming a photoresist pattern on the second hard mask layer using an ArF exposure light source in order to form a predetermined patter;

forming a first hard mask pattern by etching the second hard mask layer using the photoresist pattern as an etching mask;

etching the first hard mask layer using al least the first hard mask pattern and forming a second hard mask pattern, thereby forming a first resulting structure;

depositing an insulation layer on the first resulting structure; and

patterning the conducting layer using the second hard mask pattern as an etching mask.

14. (original) The method in accordance with claim 13, wherein the insulation layer s a flowable insulation layer or an organic polymer.

15. (original) The method in accordance with claim 13, wherein the first hard mask layer is a nitride layer and the second hard mask layer is a conducting layer which is a tungsten layer or a tungsten nitride layer.

16. (original) The method in accordance with claim 15, wherein the flowable insulation layer is a SOG layer or APL layer.

17. (original) The method in accordance with claim 14, wherein the step of removing the insulation layer and the first hard mask pattern includes the steps of:

applying a first wet etching process using a fluoride solution to remove a portion of the insulation layer;

applying a second wet etching process using an SC-1 solution to remove the first hard mask pattern; and

applying a third wet etching process using the fluoride solution to remove the residual of the first hard mask pattern.

18. (original) The method in accordance with claim 14, further comprising the step of forming an antireflective coating layer on the third hard mask layer.

19. (original) The method in accordance with claim 13, wherein the predetermined pattern is a gate electrode pattern, a bit line pattern or a metal line pattern.